REMARKS

Reconsideration of this application is respectfully requested.

Claim rejections under 35 U.S.C. §103(a)

The Action rejects Claims 1-4, 6-11, 13, 14, 16 and 17 under 35 U.S.C. §103(a) as being unpatentable over Ker et al. (U.S. Patent No. 6,521,952) in view of Lee et al. (U.S. Patent No. 6,066,879). Reconsideration and withdrawal of this rejection are respectfully requested in view of the following arguments.

To establish a *prima facie* case of obviousness, three basic criteria must be met: (a) there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings; (b) there must be a reasonable expectation of success in the combination; and (c) the prior art reference (or references when combined) must teach or suggest all the claim limitations. *See* M.P.E.P. § 706.02(j).

Applicant submits that the Action does not set forth a *prima facie* case of obviousness for Claim 1 because both Ker and Lee fail to teach or suggest "a diode string . . . coupled between a source node of the NMOS transistor [of the output buffer] and ground" recited in Claim 1 (emphasis added). As conceded by the Examiner, Ker fails to teach that the diode string 716 is coupled between a source node of the NMOS transistor and ground. Further, neither the description nor drawings of Lee teach or suggest a diode string coupled between a source node of the NMOS transistor and ground. Indeed, as best shown in Fig. 4 of Lee, the source nodes of the NMOS transistors of Lee are shorted directly to ground. Accordingly, Ker and Lee fail to teach or suggest all claim limitations of Claim 1.

Further, Applicant submits that the suggested combination of Ker and Lee does not provide a diode string coupled between a source node of the NMOS transistor and ground as recited in Claim 1. Ker's diode string 716 is coupled between the SOI-NSCR 114 and Vss, essentially in parallel with the inveter 703. The drain of the NMOS transistor of the inverter 703 is coupled to SOI-NSCR 114 and its source is coupled to the Vss. Based on Fig. 11a, the NMOS

transistor is parallel coupled to the diode string 117. With respect to Lee's FIG. 4, the DENMOS transistors Q5 and Q6 identified by the Examiner are also parallel coupled to the SCR ESD protection device. The suggested substitution of Lee's NMOS transistors and SCR ESD protection device for Ker's NMOS transistor and SOI-SCR results in a structure where the sources of the DENMOS transistors are still coupled to Vss and their drains are coupled to the SCR ESD protection device. In short, the diode string is still parallel coupled to the DENMOS transistors, rather than coupled between the source of the DENMOS transistors and ground. Accordingly, the combined teachings of Ker and Lee do not teach or suggest the claimed feature of Claim 1.

Finally, Applicant submits that there is no suggestion or motivation for one of ordinary skill in the art to replace Ker's discrete SCR and NMOS transistor with Lee's combined NMOS and SCR ESD protection device. The Action states that it would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the teachings of Ker with Lee by replacing the discrete SCR and NMOS transistor taught by Ker with the combined NMOS and SCR ESD protection device taught by Lee for the purpose of reducing the footprint of the ESD device. Applicant respectfully disagrees.

Figs. 3 and 4 of Lee show a conventional SCR ESD protection device, i.e., an ESD protection device in a conventional silicon substrate. However, Ker discloses a silicon controlled rectifier in silicon-on-insulator (SOI-SCR) as shown in Fig. 11a in order to achieve advantages of silicon-on-insulator (SOI) technology. (Lines 10-12 and 36-37, Col. 3) Ker's descriptions and drawings are substantially directed to the SOI-SCR technology. Without the SOI-SCR, the features and advantages that Ker intends to achieve cannot be accomplished. Based on Ker's Fig. 11a, the NMOS transistor of the inverter 703 referred by the Examiner is a conventional (i.e., non-SOI) NMOS transistor, rather than a SOI device. In order to achieve features described in Ker, the NMOS transistor in a conventional substrate and the SOI-SCR in a SOI substrate must be separated in different regions, i.e., the discrete SOI-SCR and NMOS transistor taught by Ker are required. Thus, one of ordinary skill in the art would not have been motivated to replace Ker's discrete SCR and NMOS transistor with Lee's combined NMOS and SCR ESD protection device, because such a replacement would have completely contravened Ker's essential features.

Accordingly, one of ordinary skill in the art would not have been motivated by the combined teachings of Ker and Lee to achieve the claimed feature of Claim 1. Therefore, it is submitted that Claim 1 and dependent Claims 2-4, 6 and 7 are allowable over the art of record.

Independent Claims 8 and 13 also recite the "a diode string . . . coupled between a source node of the NMOS transistor and ground" feature recited in Claim 1. For reasons analogous to those set forth in connection with Claim 1, it is submitted that Claims 8 and 13 are patentable over the cited combination. Claims 9-11 depend from Claim 8 and are, therefore, also patentable for at least the reasons described above. Claims 14, 16 and 17 depend from Claim 13 and are, therefore, also allowable over the art of record.

The Action also rejects Claims 5, 12, 15, 18 and 19 under 35 U.S.C. §103(a) as being unpatentable over Ker et al. (U.S. Patent No. 6,521,952) in view of Lee et al. (U.S. Patent No. 6,066,879) and further in view of Ker et al. (U.S. Patent No. 5,473,169).

Claim 5 depends from Claim 1. It is submitted that Ker's '169 patent fails to cure the deficiencies discussed above for the combined teachings of Ker's '952 patent and Lee as set forth above. Therefore, Claim 5 is patentable over the combined teachings of Ker's patents and Lee.

Claim 12 depends from Claim 8 and is, therefore, patentable for at least the reasons set forth above in connection with Claim 8.

Claims 15, 18 and 19 depend from Claim 13 and are, therefore, also patentable for at least the reasons set forth above in connection with Claim 13.

In view of the foregoing, reconsideration and withdrawal of the rejection of these claims are respectfully requested.

Conclusion

In view of the foregoing amendments and remarks, Applicant submits that this application is in condition for allowance. Early notification to that effect is respectfully requested.

The Assistant Commissioner for Patents is hereby authorized to charge any additional fees or credit any excess payment that may be associated with this communication to deposit account **04-1679.**

Respectfully submitted,

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